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TITLE: Matrix memory in virtual ground architecture

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CLAIMS:

We claim as our invention:
1. A matrix memory with memory cells that are arranged in rows and columns and that are provided for storing a logical "0" or "1", comprising:
a plurality of variable resistance resistors, each resistor arranged in one of the memory cells that stores a logical "0", each resistor also having a first, a second and a third terminal, wherein for a sequential numbering of the columns, each resistor that is arranged in an even-numbered column (even-column resistor) is characterized in that, when a first predetermined potential is applied to the first terminal of the even-column resistor and when a second predetermined potential is applied to the second terminal and when a third predetermined potential is applied to the third terminal, a resistance of the even-column resistor is so low between the first terminal and the second terminal that a compensation of the difference in potential between the first terminal and the second terminal occurs within a time provided for a read event, and wherein each even-column resistor is further characterized in that, when the first predetermined potential is adjacent the first terminal and the second predetermined potential is adjacent the second terminal and a fourth predetermined potential is adjacent the third terminal, the resistance of the even-column resistor is so high between the first terminal and the second terminal that the difference in potential between the first terminal and the second terminal is substantially preserved during the time provided for a read event, and wherein each resistor that is arranged in an odd-numbered column (odd-column resistor) is characterized in that, when the first predetermined potential is adjacent a first terminal of the odd-column resistor and when a fifth predetermined potential differing from the second predetermined potential is adjacent the second terminal and when the third predetermined potential is adjacent the third terminal, the resistance of the odd-column resistor is so low between the first terminal and the second terminal that a compensation of the difference in potential between the first terminal and the second terminal occurs within the time provided for a read event, and wherein each odd-column resistor is further characterized in that, when the first predetermined potential is adjacent the first terminal and when the fifth predetermined potential is adjacent the second terminal and when the fourth predetermined voltage is adjacent the third terminal, the resistance of the odd-column resistor is so high between the first terminal and the second terminal that the difference in potential between the first terminal and the second terminal is substantially preserved during the time provided for a read event;
a plurality of first bit lines, wherein for each pair of columns composed of an

odd-numbered column and a following even-numbered column (first pair), each first bit line electrically connecting together the first terminals of all resistors in the first pair;
a plurality of second bit lines, wherein for each pair of columns composed of an even-numbered column and a following odd-numbered column (second pair), each second bit line electrically connecting together the second terminals of all resistors in the second pair;
a plurality of word lines, each word line electrically connecting together the third terminals of all the resistors in one row;
a plurality of first switches by which the bit lines may be connected to the first predetermined potential or the second predetermined potential or the fifth predetermined potential, wherein the first predetermined potential may be applied to the first terminals of the resistors in the first pairs, wherein the second predetermined potential may be applied to the second terminals of the resistors in the even-numbered columns of the second pairs, and wherein the fifth predetermined potential may be applied to the second terminals of the resistors in the odd-numbered columns of the second pairs;
a plurality of second switches by which the word lines may be connected to the fourth predetermined potential and by which one of the word lines may be connected to the third predetermined potential; and
a plurality of third switches by which a bit line may be connected to an evaluation circuit.

2. The matrix memory as claimed in claim 1, further comprising field effect transistors as the variable resistance resistors, wherein the first terminals are drain terminals of the field effect transistors, the second terminals are source terminals of the field effect transistors and the third terminals are gate terminals of the field effect transistors.

3. The matrix memory as claimed in claim 2, further comprising n-channel MOSFETs as the field effect transistors, wherein the third predetermined potential lies above the second predetermined potential at least in the spacing of a highest threshold voltage of the field effect transistors in the even-numbered columns, and wherein the third predetermined potential lies above the fifth predetermined potential at least in the spacing of a highest threshold voltage of the field effect transistors in the odd-numbered columns.

4. The matrix memory as claimed in claim 2, further comprising p-channel MOSFETs as the field effect transistors, wherein the third predetermined potential lies below the second predetermined potential at least in the spacing of a highest threshold voltage of the field effect transistors in the even-numbered columns, and wherein the third predetermined potential lies below the fifth predetermined potential at least in the spacing of a highest threshold voltage of the field effect transistors arranged in the odd-numbered columns.

5. The matrix memory as claimed in claims 1, further comprising a grounded potential (ground) as both the second predetermined potential and the fourth predetermined potential.

6. The matrix memory as claimed in claims 1, further comprising a grounded potential (ground) as both the fifth predetermined potential and the fourth predetermined potential.

7. The matrix memory as claimed in claim 5, further comprising a difference in potential between the second predetermined potential and the fifth predetermined potential which is at least 0.3 times and at most 0.6 times the greater of either the difference in potential between the first predetermined potential and the second predetermined potential or the difference in potential between the first predetermined potential and the fifth predetermined potential.

8. The matrix memory as claimed in claim 6, further comprising a difference in potential between the second predetermined potential and the fifth predetermined potential which is at least 0.3 times and at most 0.6 times the greater of either the difference in potential between the first predetermined potential and the second predetermined potential or the difference in potential between the first predetermined potential and the fifth predetermined potential.

9. The matrix memory as claimed in claim 1, further comprising a first comparator, a second comparator and a third comparator in the evaluation circuit, wherein one input of the first comparator is connected to a first reference potential, one input of the second comparator is connected to a second reference potential and one input of the third comparator is connected to a third reference potential, and wherein other inputs of the three comparators are electrically connected to one another and to the plurality of third switches, and wherein the first reference potential lies between the second potential and a medium potential that is adjacent the first terminals of the resistors connected to one another in an odd-numbered column and the following even-numbered column when the second

predetermined potential is adjacent the second terminals of the resistors in the even-numbered column, the fifth predetermined potential is adjacent the second terminals of the resistors in the odd-numbered column and the third predetermined potential is adjacent the third terminals of at least one of the resistors that is arranged in the even-numbered column and at least one of the resistors that is arranged in the odd-numbered column, and wherein the second reference potential lies between the fifth predetermined potential and the medium potential, and wherein the third reference potential lies between the first predetermined potential and the second predetermined potential and between the first predetermined potential and the fifth predetermined potential.

10. The matrix memory as claimed in claim 9, further comprising two logic gates, the logic gates having inputs particularly connected to outputs of the three comparators such that informational content in one of two simultaneously read memory cells is represented at outputs of these gates as low or high potential.

11. The matrix memory as claimed in claim 8, further comprising an AND gate and a NAND gate as the two logic gates, wherein an inverting input of the first comparator is connected to the first reference potential, an inverting input of the second comparator is connected to the second reference potential, a non-inverting input of the third comparator is connected to the third reference potential, outputs of the first comparator and of the second comparator are connected to inputs of the AND gate, and outputs of the first comparator and of the second comparator are connected to inputs of the NAND gate.